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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,911	08/28/2001	Michael K. Gschwind	YOR9-2001-0606 (8728-545)	5165

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,911	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 7, 11 – 13, 17 – 20 and 22 – 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hao *et al.* (US Patent No. 4,569,016, hereinafter "Hao").

3. With respect to claims 1, 12 and 18, Hao discloses a method for aligning and inserting data elements into a memory based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction, comprising the steps of:

given a data item that includes a data element to be stored, aligning the data element in another memory with respect to a predetermined position in the memory, in response to the one or more alignment instructions (Rotate and Store instructions on columns 18 and 19, see also Rotate the Mask Insert instructions on column 13);

dynamically generating a mask to enable writing of a memory bit lines that correspond to the aligned data element (col. 18, lines 23 – 24); and

writing the memory bit lines to the memory under a control of the mask, wherein said generating and writing steps are performed in response to the single store instruction (col. 18, lines 24 – 27, col. 13, lines 23 – 25).

4. With respect to claims 2, 6, 19 and 20, Hao discloses a method for storing data in a memory based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction, comprising the steps of:

aligning the data in a register relative to a location of the data within a target memory address line, in response to the one or more alignment instructions (Rotate and Store instructions on columns 18 and 19, see also Rotate the Mask Insert instructions on column 13); and

storing a portion of the aligned data within the memory under a control of data type information and an address argument specified by the single store instruction, in response to the single store instruction (col. 18, lines 24 – 27, col. 13, lines 23 – 25, storing is under the control of data types, for example, immediate data for Rotate Immediate the Mask Insert instruction, and address argument, for example, Rotate then Mask Insert instruction specifies a register to store the data).

5. With respect to claim 3, the method further comprises the step of computing the mask from an address argument corresponding to the single store instruction (col. 13, 16 – 30, mask is taken from an immediate address, see also col. 18, lines 42 – 55, byte marks generated from an address is used as masks for storage of data).

6. With respect to claims 4 and 22, the address argument (col. 18, lines 26 – 28) comprises a displacement value (+4) and an address value (content of RA).

7. With respect to claims 5 and 23, the address value specifies a particular register (col. 13, lines 38 – 39).

8. With respect to claim 7, the predetermined position in the memory corresponds to a target position within a memory line (col. 20, lines 36 – 40).

9. With respect to claims 11 and 24, the instruction sequence is without a merge instruction (the steps are performed in a single Rotate and Store instructions, see also col. 13, Rotate then Mask Insert instructions).

10. With respect to claim 13, said system exploits partial line write capabilities of the memory (col. 18, lines 42 – 55, byte marks are used to partially write to a memory location).

11. With respect to claim 17, the memory comprises a cache (figure 1, 18, 20), and said means for writing writes the data element to the cache under the control of the mask (col. 3, lines 15 – 21, col. 4, lines 17 – 55, stored data is "stored in cache").

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 8 – 9 and 14 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao in view of Applicant's Admitted Prior Art (AAPA).

Hao discloses all of the limitations of the parent claims as discussed above. However, Hao does not specifically disclose the system uses data parity or ECC. On the other hand, AAPA discloses that use of data parity or ECC in a computer system is well known to those of ordinary skill in the art (specification page 11, lines 20 – 23).

It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Hao before him at the time the invention was made, to use the ECC teachings of the computer system of AAPA in the computer system of Hao, in order to order to increase the reliability of the system.

14. Claims 10, 16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao in view of Sites *et al.* (US Patent No. 6,167,509, hereinafter "Sites").

Hao discloses all of the limitations of the parent claims as discussed above. However, Hao does not specifically disclose that the method comprises the use of a read-write buffer. On the other hand, Sites discloses a method of storing data comprising a step of intermediately storing the memory bit lines from the other memory to a read-write buffer before said writing step (col. 7, lines 46 – 53).

It would have been obvious to one of ordinary skill in the art, having the teachings of Sites and Hao before him at the time the invention was made, to use the write buffer teachings of the computer system of Sites in the computer system of Hao, in order to minimize the number of CPU stall cycles by providing high bandwidth resource for receiving store data (Sites, col. 7, lines 46 – 53).

Response to Amendment

15. Claims 1, 2, 7, 10, 12, 13, 16 and 17 have been amended to overcome rejections under 35 U.S.C. 112, second paragraph. Corresponding rejections are withdrawn.

Response to Arguments

16. Applicant's arguments filed November 5, 2004 have been fully considered but they are not persuasive.

17. Applicant's first argument, that there is no positive recitation of "dynamically generating a mask to enable writing of memory bit lines" in a particular passage in column 13 in Hao cited

in the rejection even when Applicant clearly admits that the passage teaches "inserting data into another register under the control of a generated mask", is not only frivolous but also disingenuous. That particular passage, that Applicant relies on to "prove" non-anticipation, was not even cited in relation to the limitation in question in the rejection of the independent claims. The passage cited was the one in column 18, which discloses every element of the quoted limitation. But more importantly, "proving" that a particular passage in the prior art reference does not use the language identical to the language in the claim does not overcome the Examiner's prima facie case of anticipation presented in the rejection. Also, Applicant makes a general allegation without specifically pointing out what aspect of the limitation is not taught by Hao in particular. Applicant fails to offer any analysis or well-reasoned and convincing arguments as to why Hao does not teach the limitation in question. Most of Applicant's remaining arguments fail for the same reason. Applicant characterizes the anticipating features of the prior art reference in a certain way and alleges or concludes that a certain limitation is not taught. Other remaining arguments of this type will not be addressed separately. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

18. Applicant alleges that Hao does not disclose "aligning the data element in a second memory with respect to a predetermined position in the first memory." The Examiner has presumed that this limitation was meant to encompass an implementation of Applicant's invention, described in lines 1 – 9 on page 23 of the specification, that uses an alignment

network to rotate and store data. Apparently, according to Applicant's arguments, this is not the case, since Applicant argues that Hao's disclosure of rotating and storing of data does not teach this limitation. Again, Applicant does not offer any hint as to how the Examiner should interpret this limitation and does not explain why Hao's rotate and store instruction, that takes data from one memory location, rotates or aligns data bits and stores the aligned data in another memory, does not read on the claimed limitation. Since Applicant's arguments seem to indicate incorrect understanding of the claimed limitation by the Examiner, **in order to avoid rejections under 35 U.S.C. 112, first (enablement) and second (indefiniteness) paragraphs in any future Office Action, Applicant needs to fully explain what each and every significant term in the limitation means and specifically point out where in the specification enabling disclosure for each term can be found,** so that the Examiner can properly understand the limitation and conduct proper examination.

19. Applicant states "column 18 of Hao discloses storing the full merged word is [sic] into memory, contrary to Applicant's claim 19 recitation of "storing a portion of the aligned data within the memory...."" Contrary to Applicant's assertion, a full merged rotated or aligned word comprises a portion of the aligned word, hence, when a full word is stored a portion of it is stored.

20. As to Applicant's argument regarding claims 11 and 24, the claimed limitation "wherein the instruction sequence is without a merge instruction" is met because Hao's Rotate and Store

instructions are single instructions. Any merging that may occur happens within a single Rotate and Store instruction without requiring a separate merge instruction.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 17, 2004